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EXAMINER	
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ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,763	ISHIDA ET AL.	
	Examiner	Art Unit	
	Adolf DSouza	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12 and 18* is/are allowed.

6)☒ Claim(s) *1 - 5, 11, 13 - 17* is/are rejected.

7)☒ Claim(s) *6 - 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Argument: Applicant stated that Figures 1 and 3 encompassed embodiments of the invention and therefore did not label the figures as Prior Art.

Response: Examiner respectfully disagrees. Applicant has very clearly state din the specification that Figs. 1A - 1C illustrate "conventional measurement of jitter tolerance" (Specification, paragraph 4). Further, Figs. 3 only illustrates what the configuration in Fig. 2 (Prior Art) generates and therefore should be labeled as Prior Art.

2. Applicant's arguments filed 8/29/2007 have been fully considered but they are not persuasive.

Argument: Applicant has stated that independent claims 1 and 13 recite "applying jitter to a given input signal without causing an amplitude modulation component" and that neither Applicant Admitted Prior Art (AAPA) nor Trischitta teach or suggest that limitation (Remarks 8/29/2007, page 6).

Response: Examiner respectfully disagrees. Applicant's prior art Fig. 2 discloses, a deterministic jitter source 208, a sinusoidal jitter source 206 and a random jitter source 212. If the sinusoidal jitter and a random jitter were not applied and only the deterministic jitter were applied then the amplitude modulation component would not be present. Applicant's Fig 8 shows the same deterministic jitter source 104 that produces jitter without the amplitude modulation component (see Applicant's admission in

specification paragraph 97). Therefore, Examiner respectfully disagrees with Applicant that the Applicant Admitted Prior Art (AAPA) does not disclose jitter without the amplitude modulation component.

3. Applicant's arguments, see remarks (page 7), filed 8/29/2007 with respect to claims 12 and 18 have been fully considered and are persuasive. The rejection of claims 12 and 18 has been withdrawn.

Drawings

4. (a) Figures 1 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Applicant has stated that Figures 1 and 2 illustrate conventional techniques (see Description of the Drawings) and Figs. 3A – 3C just shows in more detail what is in Figure 2.

(b) The drawings are objected to because in Fig. 12, element S308, "INOUT" should be corrected to "INPUT".

See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3 – 5, 11, 13, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereafter referred to as AAPA) in view of Trischitta et al. (The Jitter Tolerance of Fiber Optic Regenerators; December 1987; IEEE Transactions on Communications; pages 1303 – 1308).

Regarding claim 1, AAPA discloses a testing device for testing an electronic device, comprising:

a deterministic jitter application unit operable to apply deterministic jitter to a given input signal without causing an amplitude modulation component and supply said input signal to said electronic device (Fig. 2, Applicant's Specification, page 2, paragraph 5 – 7; Fig. 3A – 3C; wherein the amplitude modulation component is removed by the limiting amplifier);

a jitter amount controller operable to control magnitude of said deterministic jitter generated by said deterministic jitter application unit (Applicant Specification, page 2, paragraph 5; where Applicant states that the amount of jitter applied is controlled by adjusting the amplitude of the sinusoidal jitter);

AAPA does not disclose a determination unit to measure the jitter.

In the same field of endeavor, however, Trischitta discloses a determination unit operable to determine whether or not said electronic device is defective based on an output signal output from said electronic device in accordance with said input signal (Fig. 9, everything to the right of "Optical attenuator"; section IV which gives background of how the jitter is generated and the results of jitter tolerance measurement [last paragraph in section IV; Abstract; section II and II, which shows measurement of jitter).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the jitter measurement method of Trischitta in AAPA's system because this would allow the jitter to be measured and compared the jitter tolerance template, thereby allowing one to know if the jitter is too large for the device to handle, as disclosed by Trischitta.

Regarding claim 3, AAPA discloses deterministic jitter.

AAPA not disclose said deterministic jitter application unit includes a cable operable to transmit said input signal and generate said deterministic jitter.

In the same field of endeavor, however, Trischitta discloses jitter application unit includes a cable operable to transmit said input signal and generate said jitter (page 1307, right column, 1st 3 lines; wherein cable is the long fiber span).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the fiber optic cable of Trischitta in AAPA's system because this would allow fiber optic signal to be transmitted and a test to be done for such devices, as disclosed by Trischitta.

Regarding claim 4, AAPA does not disclose magnitude of jitter is based on peak-to-peak value of alignment jitter.

In the same field of endeavor, however, Trischitta discloses jitter amount controller determines said magnitude of said deterministic jitter based on a threshold value of a peak-to-peak value of alignment jitter between said input signal and a recovered clock signal recovered by said electronic device from said input signal (page 1304, right column, 1st 10 lines).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method of Trischitta in AAPA's system because this would provide a means for the measurement of the jitter, as disclosed by Trischitta.

Regarding claim 5, AAPA discloses a sinusoidal jitter application unit operable to apply sinusoidal jitter to said input signal, wherein said jitter amount controller further controls magnitude of said sinusoidal jitter generated by said sinusoidal jitter application unit

(Applicant's Figure 2, element 206; Specification, page 2, paragraph 5 which states that the amplitude of the sinusoidal jitter is changed).

Regarding claim 6, AAPA does not disclose the magnitude of sinusoidal jitter is based on peak-to-peak value of alignment jitter.

In the same field of endeavor, however, Trischitta discloses jitter amount controller determines said magnitude of said sinusoidal jitter based on a threshold value of a peak-to-peak value of alignment jitter between said input signal and a recovered clock signal recovered by said electronic device from said input signal, and a jitter transfer function in a nondefective electronic device (page 1305, right column, last paragraph before section III, 1st 2 lines; page 1306, right column, para starting with "In the previous section ..." – paragraph ending with " ...model of section I; wherein the jitter transfer functions is as state din Equation 17 and 18).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method of Trischitta in AAPA's system because this would provide a means for the measurement of sinusoidal jitter, as disclosed by Trischitta.

Regarding claim 11, AAPA does not disclose using a reference clock signal for sampling the input signal.

In the same field of endeavor, however, Trischitta discloses the electronic device receives said input signal and a reference clock signal as its input and samples said

input signal based on said reference clock signal wherein said testing device further comprises a phase shifter operable to shift a phase of said reference clock signal (Fig. 1; page 1303, right column, paragraph starting with "The received signal is sampled... " to page 1304, left column, paragraph ending with "... sampled at an optimum time"; wherein the input signal is received from the incoming fiber and the reference clock signal after being obtained from the retiming circuit, is used to sample the input signal and the phase shifter is done either by choosing the length of the coaxial cable or the electronic phase shifting network).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method of Trischitta in AAPA's system because this would provide a means for optimum sampling of the input data, as disclosed by Trischitta.

Claims 13, 15 and 16 are directed to method/steps of the same subject matter claimed in apparatus claims 1, 3 and 5 respectively and therefore, are rejected as explained in the rejections of claims 1, 3 and 5 above.

7. Claims 2, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereafter referred to as AAPA) in view of Trischitta et al. (The Jitter Tolerance of Fiber Optic Regenerators; December 1987; IEEE Transactions

on Communications; pages 1303 – 1308) and further in view of Anderson et al. (US 5,793,822).

Regarding claim 2, AAPA does not disclose the deterministic jitter application unit includes a primary filter.

In the same field of endeavor, however, Anderson discloses deterministic jitter application unit includes a primary filter operable to transmit said input signal and generate said deterministic jitter (Fig. 1, elements 13, 11, 17; column 3, lines 2 – 55, 48 - 49; wherein the jitter injection circuit is element 13 that injects jitter into PLL 11 which uses the filter 17 and the deterministic jitter is the known sinusoidal jitter).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method of Anderson in AAPA's system because this would provide a means for generating controlled sinusoidal jitter, as disclosed by Anderson.

Claim 14 is directed to method/steps of the same subject matter claimed in apparatus claim 2 and therefore, is rejected as explained in the rejection of claim 2 above.

8. Claims 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereafter referred to as AAPA) in view of Trischitta et al. (The Jitter Tolerance of Fiber Optic Regenerators; December 1987; IEEE Transactions

on Communications; pages 1303 – 1308) and further in view of Yamaguchi et al. (US 20030202573).

Regarding claim 17, AAPA does not disclose sinusoidal jitter of multiple frequency components.

In the same field of endeavor, however, Yamaguchi discloses sinusoidal jitter application unit applies said sinusoidal jitter having a plurality of frequency components to said input signal (paragraph 28).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method of Yamaguchi in AAPA's system because this would provide a means for having sinusoidal jitter of multiple frequencies, as disclosed by Yamaguchi.

Allowable Subject Matter

9. Claims 12 and 18 are allowed.

The following is an examiner's statement of reasons for allowance: Regarding claims 12 and 18, the prior art fails to disclose that the jitter amount controller determines said magnitude of said sinusoidal jitter based on a threshold value of a peak-to-peak value of alignment jitter between said input signal and a recovered clock signal recovered by

said electronic device from said input signal, and a jitter transfer junction in said electronic device that is nondefective.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

10. Claims 6 - 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Prior Art Cited

The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to jitter measurement:

Cupo (US 4,847,864) discloses a phase jitter compensation arrangement using an adaptive IIR filter.

Mesuda et al. (US 5,563,921) discloses a Jitter detection apparatus using double-PLL structure.

Dalmia et al. (US 5,835,501) discloses a built-in test scheme for a jitter tolerance test of a clock and data recovery unit.

Fala et al. (US 20030048500) discloses a Method and apparatus for testing network integrity.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf DSouza whose telephone number is 571-272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

AD

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER